CLAIMS

1. A semiconductor device comprising:

a semiconductor substrate;

a silicon carbide layer formed on the semiconductor substrate and having its top surface inclined at an angle of 10 degrees or less from a crystal plane in a miscut direction;

a gate insulating film formed on the silicon carbide layer;

a gate electrode formed on the gate insulating film;

a source electrode formed on a part of the silicon carbide layer located to a side of the gate electrode;

a drain electrode formed on the back surface of the semiconductor substrate; and

a source region formed in a region of the silicon carbide layer located at least under the source electrode,

wherein the longest of the edges of the source region extends along the direction perpendicular to the miscut direction in a plan view.

2. The semiconductor device of Claim 1, further comprising:

a well region of a second conductivity type formed in a part of the silicon carbide layer located on a lateral side of the source region and under the source region; and

a base electrode electrically connected to the well region.

3. The semiconductor device of Claim 1, wherein

a direction extending along the direction perpendicular to the miscut direction is a direction at an inclination of 5 degrees or less from the direction perpendicular to the miscut direction.

4. The semiconductor device of Claim 1, wherein

a channel layer is formed in a region of the silicon carbide layer located under the gate insulating film.

5. The semiconductor device of Claim 4, wherein

the channel region has a multilayer structure including a first silicon carbide layer of at least one layer and a second silicon carbide layer of at least one layer having a higher first-conductivity-type dopant concentration and a smaller thickness than the first silicon carbide layer.

6. The semiconductor device of Claim 1, wherein

the electron mobility through the silicon carbide layer is larger in the direction perpendicular to the crystal plane than in in-plane directions of the crystal plane.

7. The semiconductor device of Claim 1, wherein

the silicon carbide layer is 4H-SiC.

8. The semiconductor device of Claim 1, wherein

the top surface of the silicon carbide layer is a plane inclined from the (0001) plane in the <11-20> direction.

9. The semiconductor device of Claim 1, wherein

the top surface of the silicon carbide layer is a plane inclined from the (0001) plane in the <1-100> direction.

10. The semiconductor device of Claim 1, wherein

the gate insulating film is formed by thermally oxidizing the upper part of the silicon carbide layer and subjecting the resultant upper part thereof to heat treatment in an atmosphere containing a compound inclusive of a group-V element.

11. The semiconductor device of Claim 10, wherein

the compound inclusive of the group-V element is nitric oxide.

12. The semiconductor device of Claim 10, wherein

a maximum nitrogen concentration is 1×10^{20} cm^{-3} through 1×10^{22} cm^{-3} both inclusive at the interface between the silicon carbide layer and the gate insulating film.

13. The semiconductor device of Claim 1, wherein

the source electrode is formed using the same conductive film as the base electrode.

14. The semiconductor device of Claim 1, wherein

the gate electrode is formed to have a shape in which polygons are hollowed out in a plan view, and

the longest of the edges of the hollowed polygons extend along the direction perpendicular to the miscut direction.

15. The semiconductor device of Claim 14, wherein

the source electrode is formed in the shape of polygons in a plan view, and

the gate electrode is formed so as to be located apart from the source electrode and surround the lateral sides of the source electrode.

16. The semiconductor device of Claim 1, wherein

the gate electrode is formed in the shape of a polygon in a plan view, and

the longest of the edges of the polygon extends along the direction perpendicular to the miscut direction.

17. The semiconductor device of Claim 16, wherein

in a plan view, the source electrode is formed to have a comb shape including a plurality of first rectangular parts arranged in stripes and a first connection part through which the respective one ends of the plurality of first rectangular parts are connected to one another, and the gate electrode is formed to have a comb shape including a plurality of striped second rectangular parts arranged alternately with the plurality of first rectangular parts and a second connection part through which the respective one ends of the plurality of second rectangular parts are connected to one another.

18. A semiconductor device comprising:

a semiconductor substrate;

a silicon carbide layer formed on the semiconductor substrate and having its top surface inclined at an angle of 10 degrees or less from a crystal plane in a miscut direction;

a gate insulating film formed on the silicon carbide layer;

a gate electrode formed on the gate insulating film;

a source electrode formed on a part of the silicon carbide layer located to one side of

the gate electrode;

a drain electrode formed on a part of the silicon carbide layer located to the other side of the gate electrode; and

source/drain regions formed apart from each other in regions of the silicon carbide layer located at least under the source and gate electrodes,

wherein the opposed two of the edges of the source/drain regions extend along the direction perpendicular to the miscut direction in a plan view.

19. The semiconductor device of Claim 18, further comprising:

a base region formed in the silicon carbide layer and containing dopants of a first conductivity type; and

a base electrode electrically connected to the base region.

20. The semiconductor device of Claim 18, wherein

the gate electrode is formed in the shape of a polygon, and

the longest of the edges of the polygon extends along the direction perpendicular to the miscut direction.

21. The semiconductor device of Claim 18, wherein

a direction extending along the direction perpendicular to the miscut direction is a direction at an inclination of 5 degrees or less from the direction perpendicular to the miscut direction.

22. The semiconductor device of Claim 18, wherein

a channel layer is formed in a region of the silicon carbide layer located under the gate insulating film.

23. The semiconductor device of Claim 22, wherein

the channel region has a multilayer structure including a first silicon carbide layer of at least one layer and a second silicon carbide layer of at least one layer having a higher first-conductivity-type dopant concentration and a smaller thickness than the first silicon carbide layer.

24. The semiconductor device of Claim 18, wherein

the electron mobility through the silicon carbide layer is larger in the direction perpendicular to the crystal plane than in in-plane directions of the crystal plane.

25. The semiconductor device of Claim 18, wherein

the silicon carbide layer is 4H-SiC.

26. The semiconductor device of Claim 18, wherein

the top surface of the silicon carbide layer is a plane inclined from the (0001) plane in the <11-20> direction.

27. The semiconductor device of Claim 18, wherein

the top surface of the silicon carbide layer is a plane inclined from the (0001) plane in the <1-100> direction.

28. The semiconductor device of Claim 18, wherein

the gate insulating film is formed by thermally oxidizing the upper part of the silicon carbide layer and subjecting the resultant upper part thereof to heat treatment in an atmosphere containing a compound inclusive of a group-V element.

29. The semiconductor device of Claim 28, wherein

the compound inclusive of the group-V element is nitric oxide.

30. The semiconductor device of Claim 28, wherein

a maximum nitrogen concentration is 1×10^{20} cm^{-3} through 1×10^{22} cm^{-3} both inclusive at the interface between the silicon carbide layer and the gate insulating film.

31. The semiconductor device of Claim 18, wherein

the source electrode is formed using the same conductive film as the base electrode.